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Prior application Serial No.: 09/383,523

Examiner: Kimberly White

Art Unit: 2811

ASSISTANT COMMISSIONER FOR PATENTS

Washington, DC 20231

SIR: This is a request for filing a ☐ continuation ☒ divisional application under 37 CFR Section 1.53(b) of pending prior application Serial No. 09/383,523 filed on July 29, 1999 of JAMMY et al for METHOD FOR FORMING CRYSTALLINE SILICONE NITRIDE

1. ☒ Enclosed is a complete copy of the prior application, including the oath or declaration as originally filed.

2. ☒ The filing fee is calculated below:

CLAIMS AS FILED HEREIN AFTER ANY ACCOMPANYING
PRELIMINARY AMENDMENT

For:	No. filed	No. extra
Basic Fee:		
Total Claims	3 - 20 =	0
Independent Claims	1 - 3 =	0
<input type="checkbox"/> Multiple Dependent Claim Presented		

*If the difference in Col. 1 is less than zero, enter "0" in Col. 2.

Fees for small entity		OR	Fees for other than a small entity	
Rate	Fee		Rate	Fee
	\$345.00		OR	\$690.00
x \$9.00 =	\$		OR	x \$18.00 = \$ 0.00
x \$39.00 =	\$		OR	x \$78.00 = \$ 0.00
+ \$130.00 =	\$		OR	+ \$260.00 = \$ 0.00
Total	\$		OR	Total \$690.00

3. ☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Account No. 19-2179. A duplicate copy of this sheet is enclosed.

4. ☒ Cancel in the application original claims 1-17 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

5. ☒ Amend the specification by inserting before the first line the sentence:

--This is a ☐ continuation, ☒ divisional, of application serial no. 09/383,523 filed on July 29 --

6. ☒ The prior application is assigned of record to Siemens Aktiengesellschaft.

7. ☐ The power of attorney in the prior application is to

a. ☒ The power appears in the original papers in the prior application.

09/09/00 15:04:00

b. [] Since the power does not appear in the original papers, a copy of the power in the prior application is enclosed.

c. [X] Address all future communications to:

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
Iselin, NJ 08830

Address all telephone calls to: Elsa Keller, Legal Administrator (732) 321-3026.

8. [] A Preliminary Amendment is enclosed. (Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.)

9. [X] I hereby declare that the attached papers are a true copy of the prior application serial no. 09/383,523 filed on July 29.

10. [X] I hereby appoint each and every one of the below-named individuals as my associate, each to have full power to prosecute the referenced case and any continuations thereof and to take any action regarding the above-referenced case which I could take, with the same force and effect as if it had been taken by me:

Adel A. Ahmed	Reg. No. 29,606	Jeffrey P. Morris	Reg. No. 25,307
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Erik Swanson	Reg. No. 40,194	Stuart Kaler	Reg. No. 35,913
I. Marc Asperas	Reg. No. 37,274		

11. [X] The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-2179. A duplicate copy of this paper is enclosed.

a. [X] Any additional filing fees required under 37 CFR Section 1.16.

b. [X] Any patent application processing fees under 37 CFR Section 1.17.

12. [X] The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 19-2179. A duplicate copy of this paper is enclosed.

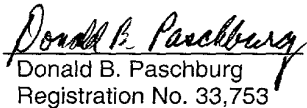
a. [X] Any patent application processing fees under 37 CFR Section 1.17.

b. [X] Any filing fees under 37 CFR Section 1.16 for presentation of extra claims.

13. [X] Please make of record and consider in the present Application the prior art of record in the prior application.

Respectfully submitted,

Date: June 15, 2000


Donald B. Paschburg
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APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

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TITLE OF INVENTION: METHOD FOR FORMING CRYSTALLINE NITRADE

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

METHOD FOR FORMING CRYSTALLINE SILICON NITRIDE

BACKGROUND

5 1. Technical Field

This disclosure relates to semiconductor fabrication and more particularly, to a method for forming crystalline silicon nitride dielectric layers for semiconductor devices.

10

2. Description of the Related Art

15 Silicon nitride is used extensively in microelectronic technology for its superior dielectric properties. Typically, silicon nitride includes superior dielectric constant (e.g., $\epsilon = 7.5$ for silicon nitride) as compared to silicon dioxide (e.g., $\epsilon = 3.9$). The need for higher capacitance with shrinking dimensions in semiconductor devices such as dynamic random access memories (DRAMs) has been met by reducing the thickness
20 of dielectric layers. Much of the silicon nitride employed for microelectronic applications is deposited by Chemical Vapor Deposition (CVD) techniques and is amorphous in structure. Although thick amorphous silicon nitride (Si_3N_4) films have adequately low leakage
25 currents, for thin ($< 50 \text{ \AA}$) dielectric films, higher leakage currents impede, if not preclude, successful device implementation.

To overcome the limitations posed by excessive

leakage currents observed in thin CVD nitride dielectric layers, a thermally grown Si_3N_4 component is added to the CVD nitride layer. Thermally grown Si_3N_4 is denser than CVD silicon nitride and exhibits superior electrical properties for the same thickness. However, thermal growth of silicon nitride is a self limiting process (at about 950 °C approximate thickness of nitride layer is 18-23 Å which is limited by the thermal growth process). To meet the total required thickness, a CVD nitride layer may be added to the initial thermal nitride.

For DRAM chips employing deep trench capacitors, a node dielectric is deposited in a deep trench. The node dielectric separates the storage node in the deep trench from a buried plate outside the trench to form a capacitor. It is desirable for the node dielectric to be as thin as possible to provide a high capacitance with minimal or low leakage. Node dielectrics have evolved from using an oxide only (O) dielectric layer to a mixed oxide-nitride (ONO) and currently to nitride-oxide (NO) dielectric layers to take advantage of the higher ϵ of Si_3N_4 . Similarly, for gate dielectrics, in addition to a reduction in thickness, incorporation of some nitride into the oxide film is being explored to boost the physical thickness (and dielectric constant) while keeping the equivalent oxide thickness small enough to meet the needs of smaller and faster devices.

A desirable option for improving the properties

of ultra-thin dielectric layers would be to employ crystalline Si_3N_4 films for such applications. Unlike CVD nitride films, in which the large leakage currents have been attributed to the presence of a large number of defects and pinholes, crystalline nitride films by nature could be denser and relatively defect free. However, crystalline Si_3N_4 films are difficult to grow and unstable due to lattice mismatch with silicon and the consequent excessive strain at the growth interface. An added complication for the case of a node dielectric is the presence of a thin non-stoichiometric native oxide on the exposed silicon surface of a substrate which inhibits the reaction between nitridizing species and the silicon substrate. This native oxide may be partially responsible for the electrical leakage in thermally grown nitride films.

Therefore, a need exists for a method to preclean and remove a native oxide before thermal nitridation of exposed silicon is performed. A further need exists for a method for forming a crystalline silicon nitride for semiconductor devices.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method for forming a crystalline silicon nitride layer, includes the steps of providing a crystalline silicon substrate with an exposed silicon surface, precleaning

the exposed surface by annealing in a hydrogen ambient and further annealing or exposing the exposed surface to nitrogen (e.g. in an ammonia ambient) to form a crystalline silicon nitride layer.

5 A method for forming a node dielectric layer in deep trenches, includes the steps of providing a crystalline silicon substrate with trenches formed therein, the trenches including surfaces with exposed silicon, precleaning the exposed silicon surfaces by
10 employing a hydrogen prebake, exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer, depositing an amorphous silicon nitride layer over the crystalline silicon nitride layer, and oxidizing the amorphous silicon nitride layer to form a node (NO)
15 dielectric layer.

 In alternate methods, the step of precleaning may include the step of employing a wet cleaning process to remove native oxide from the exposed surface(s). The cleaning process may include HF cleaning. The step of
20 precleaning may include the step of prebaking the exposed surface(s), in situ, in the presence of hydrogen gas, hydrogen plasma or similar reducing atmospheres at a temperature between about 400 °C and about 1300 ° at a pressure between about 10^{-9} Torr and about 600 Torr. The
25 step of precleaning may include the step of prebaking the exposed surface(s) in the presence of hydrogen gas introduced at a flow rate of between about 100 sccm and about 20 SLM for between about 2 seconds and about 3600

seconds. Flow rates and time durations can vary over a wide range of acceptable values depending on the conditions and the tool set employed. The step of annealing/exposing the exposed surface(s) to nitrogen to form a crystalline silicon nitride layer may include the step of introducing ammonia at a temperature of between about 400 °C and about 1300 °C. The step of exposing the exposed surface(s) to nitrogen to form a crystalline silicon nitride layer may include the step of maintaining ammonia at a pressure of between about 10^{-6} Torr and about one atmosphere or greater. A semiconductor device may be fabricated in accordance with the methods described herein.

A trench capacitor, in accordance with the present invention, includes a crystalline silicon substrate including deep trenches having surfaces substantially free of native oxide. A dielectric stack, including a crystalline silicon nitride layer, is formed on the surfaces of the trenches. The dielectric stack forms a node dielectric between electrodes of the trench capacitor.

In alternate embodiments, the crystalline silicon nitride layer may include a thickness of between about 3 Å and about 40 Å. The dielectric stack may include an oxidized amorphous nitride layer.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative

embodiments thereof, which is to be read in connection with the accompanying drawings.

5 BRIEF DESCRIPTION OF DRAWINGS

 This disclosure will present in detail the following description of preferred embodiments with reference to the following figures wherein:

 FIG. 1 is a flow diagram showing a method for
10 forming a crystalline silicon nitride layer in accordance with the present invention;

 FIG. 2 is a cross-sectional view of a trench formed in a silicon substrate for forming a silicon nitride crystalline layer in accordance with the present
15 invention;

 FIG. 3 is a magnified cross-sectional view of area 8 of FIG. 2 showing a crystalline silicon nitride layer formed in accordance with the present invention;

 FIG. 4 is a cross-sectional view of the area 8
20 of FIG. 3 showing an additional silicon nitride layer formed in accordance with the present invention; and

 FIG. 5 is a cross-sectional view of the area 8 of FIG. 4 showing an oxidized silicon nitride layer formed in accordance with the present invention.

25

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

 The present invention relates to semiconductor fabrication and more particularly, to a method for

forming crystalline silicon nitride dielectric layers for semiconductor devices. Silicon nitride, and preferably stoichiometric Si_3N_4 , is an important dielectric material for many microelectronic applications needing a high dielectric constant (ϵ) with low leakage currents. Much of the silicon nitride used for such applications is amorphous and is typically a combination of both thermally grown (in N_2 or NH_3) and/or deposited (by LPCVD techniques) materials. Although desirable for their enhanced properties, crystalline silicon nitride films are difficult to grow due to lattice mismatch and off-stoichiometric growth kinetics. The present invention includes a method for forming a crystalline silicon nitride layer. In a preferred embodiment the present invention is illustratively described for the formation of a node dielectric in deep trenches for deep trench capacitors. Other applications are contemplated as well. A preclean process is desirable prior to the formation of the crystalline silicon nitride layer.

Referring now in specific detail to the drawings in which like reference numerals identify similar or identical elements throughout the several views, and initially to FIGS. 1 and 2, a flow diagram for a method in accordance with the invention (FIG. 1) and a cross-sectional view of a semiconductor chip 10 (FIG. 2) are shown. Semiconductor chip 10 may include a memory device such as, a dynamic random access memory (DRAM), a synchronous DRAM (SDRAM), static RAM or other memory

device. It is to be understood that the present invention is not limited to semiconductor memories. The invention may be practiced for semiconductor chips which may include processors, embedded DRAM or other embedded memory devices, application specific integrated circuit chips (ASIC) or any other devices which employ dielectric films.

Semiconductor chip 10 of FIG. 2, illustratively shows a semiconductor memory having deep trench capacitor technology. In block 1, a semiconductor chip 10 is provided. Semiconductor chip 10 includes a substrate 12 which may be a monocrystalline silicon substrate, however, other silicon based/modified materials may be employed, for example, silicon on insulator, epitaxially grown silicon, etc. A pad stack 11 is formed on substrate 12. Pad stack 11 preferably includes a thermal oxide layer 13 and a pad nitride layer 15. Deep trenches 14 have been formed in substrate 12 by methods known to those skilled in the art. A buried plate 16 is also formed by conventional methods. These methods may include depositing arsenic silicate glass (ASG) in the trench as a dopant source and diffusing dopants into substrate 12. Alternate techniques may include employing ion bombardment or gas phase doping to form buried plate 16.

Prior to further processing, it is preferable to preclean exposed surfaces of substrate 12, i.e., trench sidewalls, to remove native oxides which may form

on the surface of substrate 12. In block 2, a standard cleaning process is performed to remove the native oxide on the trench sidewalls and exposed surfaces. The cleaning process may include a wet cleaning process, such as, a HF clean or other cleaning processes known in the art, such as, a RCA/B clean. Combinations of cleaning processes may also be employed. The wafers or chips are then transferred to the reaction chamber for further processing. The reaction chamber in which processing occurs is then evacuated if the transfer is not done, in situ, under vacuum..

In block 3, a hydrogen (H_2) preclean is performed on the exposed silicon surface of the trench sidewalls after the evacuation of the reaction chamber. This step further removes the native oxide from the silicon surface of substrate 12 at sidewalls of trench 14. The efficacy of the clean process depends on the temperature, time, gas flow and pressure. In a preferred method, the gas flow may include a flow rate of about 100 sccm and about 10 SLM for between about 2 seconds and about 3600 seconds. Flow rates and time durations can vary over a wide range of acceptable values depending on the conditions and the tool set employed. The step of precleaning may include the step of prebaking exposed silicon surface(s), in situ, in the presence of hydrogen gas, hydrogen plasma or similar reducing atmospheres at a temperature between about 400 °C and about 1300 ° and at a pressure between about 10^{-9} Torr and about 600 Torr.

FIG. 2 indicates an area of interest 8 which is magnified in FIGS. 3, 4 and 5 to show the process step of the method of the present invention.

Referring to FIG. 3, with continued reference to FIG. 1, after evacuating the reaction chamber of any H_2 (typical but not necessary), the silicon surface of substrate 12 is exposed to nitrogen containing compounds, preferably ammonia (NH_3) or N_2 gas, in block 4. For convenience, the process will be illustratively described using ammonia. The nitrogen may be introduced with other materials or compounds, for example, N_2 gas, atomic nitrogen formed by plasma techniques or nitrogen containing organic or inorganic precursors. Ammonia is preferably introduced into the reaction chamber at a temperature of between about 400 °C and about 1300 °C, preferably between about 900 °C and about 1100 °C. The pressure maintained in the chamber during the introduction of the ammonia is between about 10^{-6} Torr and about one atmosphere or greater, preferably between about 1 Torr and about 600 Torr. The thickness of a nitride layer 18 formed during this step is largely dependent on the temperature and to a lesser extent on the pressure. In a preferred embodiment, a thickness of nitride layer 18 is between about 3 Å to about 40 Å. Nitride layer 18 forms a crystalline silicon nitride layer.

The crystalline characteristics of this nitride layer 18 have been confirmed by tests and analysis. For example, a substantially continuous crystalline silicon

nitride layer was observed along the trench sidewalls of a semiconductor device. Nitride layer 18 exhibited characteristics indicative of a crystalline layer and was uniformly oriented parallel to the silicon in the sidewalls of the trench. Measurement of the lattice planes of nitride layer 18 resulted in a measured spacing of approximately 4 Å, which is a close match to the theoretical spacing of 3.88 Å for the (110) planes of hexagonal Si₃N₄.

Nitride layer 18 may include a thickness of between 2-6 atomic layers. In addition, analysis on a Scanning Transmission Electron Microscope (STEM) with a 2-3 Å lateral resolution and Electron Energy Loss Spectroscopy (EELS) with an energy resolution of 0.35 eV confirmed that the layer was crystalline silicon nitride and oxide at the silicon to silicon nitride interface was absent. The crystalline silicon nitride layer was not observed when the sample was not subjected to in situ H₂ pre-bake and NH₃ nitridation in accordance with the present invention.

The H₂ pre-bake, in block 3, results in a thicker nitride layer 18. Depending on the growth conditions (i.e, crystal directions of the surface on which the film is to be grown), the pressure of the H₂ pre-bake (block 3) and the time between the cleaning (block 2) and H₂ pre-bake (block 3) three distinct types of nitride films may result. The three distinct types of nitride films are illustratively described in terms of

specifics. These specifics are not to be construed as limiting as other parameters may be employed in accordance with the invention to achieve similar results. The three distinct types of nitride films that may result include:

a) a continuous crystalline layer which is formed if the pressure is about 5 Torr and the amount of time between the cleaning process and the H₂ pre-bake is between less than about 30 seconds and about 1 hour;

b) a floating (partial) crystalline layer is formed if the pressure is below about 5 Torr and the amount of time between the cleaning process and the H₂ pre-bake is between more than about 1 hour; and

c) an amorphous layer is formed outside the parameters of a) and b).

Advantageously, this provides the ability to modulate silicon nitride layer 18 by varying the process conditions. Other process parameters and tool settings may be used as well.

Referring to FIG. 4 with continued reference to FIG. 1, an additional silicon nitride layer 20 may be deposited by a chemical vapor deposition (CVD) process or a physical vapor deposition process in block 5, to obtain a desired thickness of a total dielectric layer. The total dielectric layer thickness is comprised of nitride layer 18 and nitride layer 20.

Referring to FIG. 5 with continued reference to FIG. 1, an additional step may be performed to make the

total dielectric layer compatible with later processes. Nitride layers 18 and 20 may be exposed to an oxidizing ambient at suitable temperatures to form an oxidized portion of nitride layer 20 thereby forming an N-O stack.

5 Processing then continues as is known in the art. A storage node is formed in trench by filling the trench with polysilicon. The storage node (not shown) and buried plate 16 act as capacitor electrodes for which the N-O stack is the capacitor or node dielectric.

10 Although described in terms of a deep trench capacitor, the present invention may be applied to other semiconductor structures and devices. For example, the crystalline silicon nitride layer may be employed instead of a gate oxide for vertical transistors. Other
15 applications are contemplated as well. Local nitride crystallization may also be formed by employing the above methods in accordance with the present invention. For example, localized nitride crystals may be formed on polycrystalline silicon surfaces to provide a dielectric
20 layer thereon. This embodiment may be employed for forming devices in flash memories, for example, or other devices employing polysilicon.

Having described preferred embodiments for a method for forming crystalline silicon nitride (which are
25 intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes

may be made in the particular embodiments of the invention disclosed which are within the scope and spirit of the invention as outlined by the appended claims.

Having thus described the invention with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A method for forming a crystalline silicon nitride layer, comprising the steps of:

5 providing a crystalline silicon substrate with an exposed surface;

precleaning the exposed surface by employing a hydrogen prebake; and

10 exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer.

2. The method as recited in claim 1, wherein the step of precleaning includes the step of employing a hydrogen fluoride wet clean process to remove native oxide from the exposed surface.

15 3. The method as recited in claim 2, wherein the step of precleaning the exposed surface by employing a hydrogen prebake is delayed from the step of employing a hydrogen fluoride wet clean process to remove native
20 oxide from the exposed surface by an interval of between about 30 seconds and about 3600 seconds.

4. The method as recited in claim 1, wherein the step of precleaning includes the step of prebaking the
25 exposed surface in the presence of hydrogen gas at a temperature between about 400 °C and about 1300 °C.

5. The method as recited in claim 1, wherein the step of precleaning includes the step of prebaking the exposed surface in the presence of hydrogen gas at a pressure between about 10^{-9} Torr and about 600 Torr.

5

6. The method as recited in claim 1, wherein the nitrogen includes at least one of nitrogen gas, ammonia, atomic nitrogen plasma, an organic nitrogen precursor and an inorganic nitrogen precursor.

10

7. The method as recited in claim 1, wherein the step of exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer includes the step of introducing ammonia at a temperature of between about 400 °C and about 1300 °C.

15

8. The method as recited in claim 1, wherein the step of exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer includes the step of maintaining ammonia at a pressure of between about 10^{-6} Torr and about one atmosphere.

20

9. A semiconductor device fabricated in accordance with the method as recited in claim 1.

25

10. A method for forming a node dielectric layer in

deep trenches, comprising the steps of:

providing a crystalline silicon substrate with trenches formed therein, the trenches including exposed silicon surfaces;

5 precleaning the exposed surfaces by employing a hydrogen prebake;

 exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer;

 depositing an amorphous silicon nitride layer over
10 the crystalline silicon nitride layer; and

 oxidizing the amorphous silicon nitride layer to form a node dielectric layer.

 11. The method as recited in claim 10, further comprising the step of employing a hydrogen fluoride
15 clean process to remove native oxide from the exposed surfaces.

 12. The method as recited in claim 11, wherein the step of precleaning the exposed surfaces by employing a
20 hydrogen prebake is delayed from the step of employing a hydrogen fluoride clean process to remove native oxide from the exposed surfaces by an interval of between about 30 seconds and about 3600 seconds.

 25 13. The method as recited in claim 10, wherein the step of precleaning includes the step of prebaking the

exposed surfaces in the presence of hydrogen gas at a temperature between about 400 °C and about 1300 °C.

14. The method as recited in claim 10, wherein the
5 step of precleaning includes the step of prebaking the exposed surfaces in the presence of hydrogen gas at a pressure between about 10^{-9} Torr and about 600 Torr.

15. The method as recited in claim 10, wherein the
10 step of exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer includes the step of introducing the ammonia at a temperature of between 400 °C and about 1300 °C.

15 16. The method as recited in claim 10, wherein the step of exposing the exposed surfaces to ammonia to form a crystalline silicon nitride layer includes the step of maintaining the ammonia at a pressure of between about 10^{-6} Torr and about one atmosphere.

20

17. A semiconductor device fabricated in accordance with the method as recited in claim 10.

18. A trench capacitor comprising:
25 a crystalline silicon substrate including deep trenches having surfaces in the substrate substantially

free of native oxide; and

a dielectric stack, including a crystalline silicon nitride layer, formed on the surfaces of the trenches, the dielectric stack for forming a node dielectric between electrodes of the trench capacitor.

19. The trench capacitor as recited in claim 18, wherein the crystalline silicon nitride layer includes a thickness of between about 3 Å and about 40 Å.

20. The trench capacitor as recited in claim 18, wherein the dielectric stack includes an oxidized amorphous nitride layer.

ABSTRACT OF THE DISCLOSURE

In accordance with the present invention, a method for forming a crystalline silicon nitride layer, includes the steps of providing a crystalline silicon substrate with an exposed surface, precleaning the exposed surface by employing a hydrogen prebake and exposing the exposed surface to nitrogen to form a crystalline silicon nitride layer. Also, a trench capacitor, in accordance with the present invention, includes a crystalline silicon substrate including deep trenches having surface substantially free of native oxide. A dielectric stack, including a crystalline silicon nitride layer, is formed on the sidewalls of the trenches. The dielectric stack forms a node dielectric between electrodes of the trench capacitor.

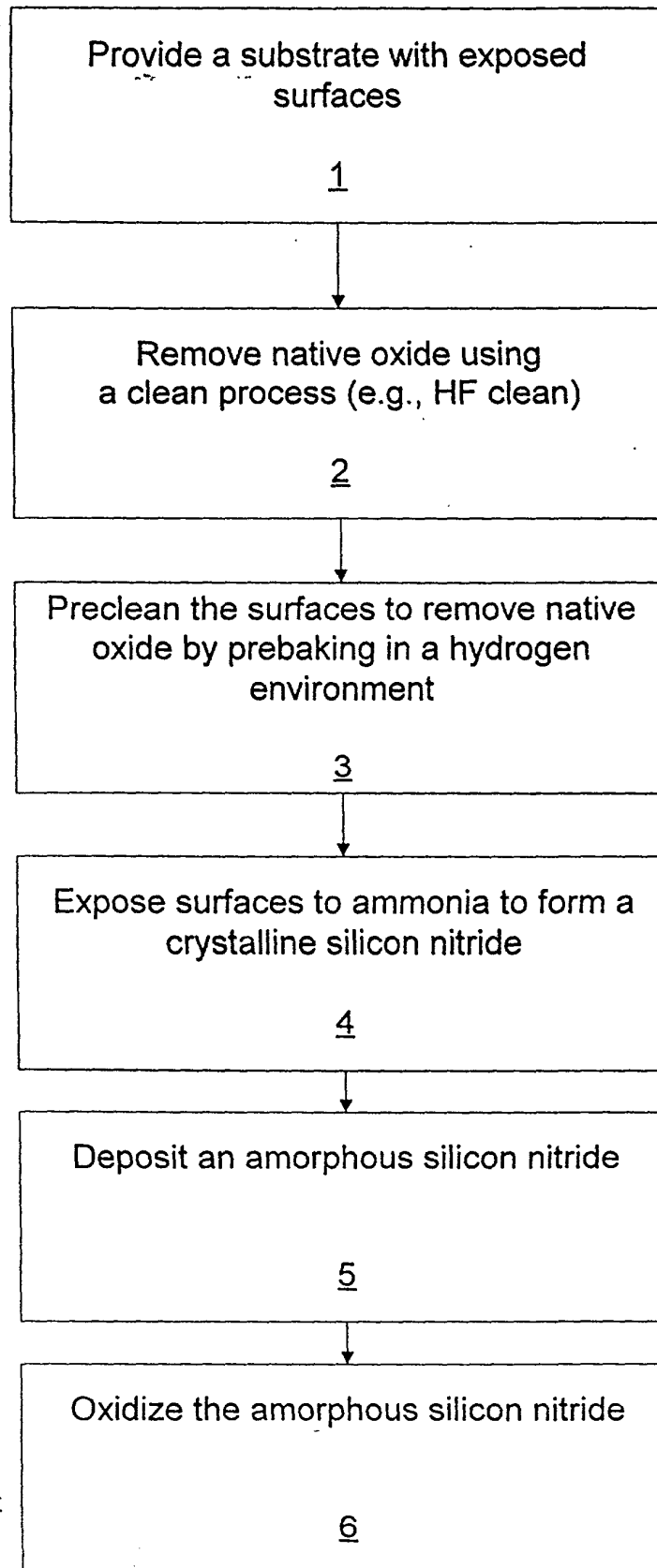


FIG. 1

10 ~ ~

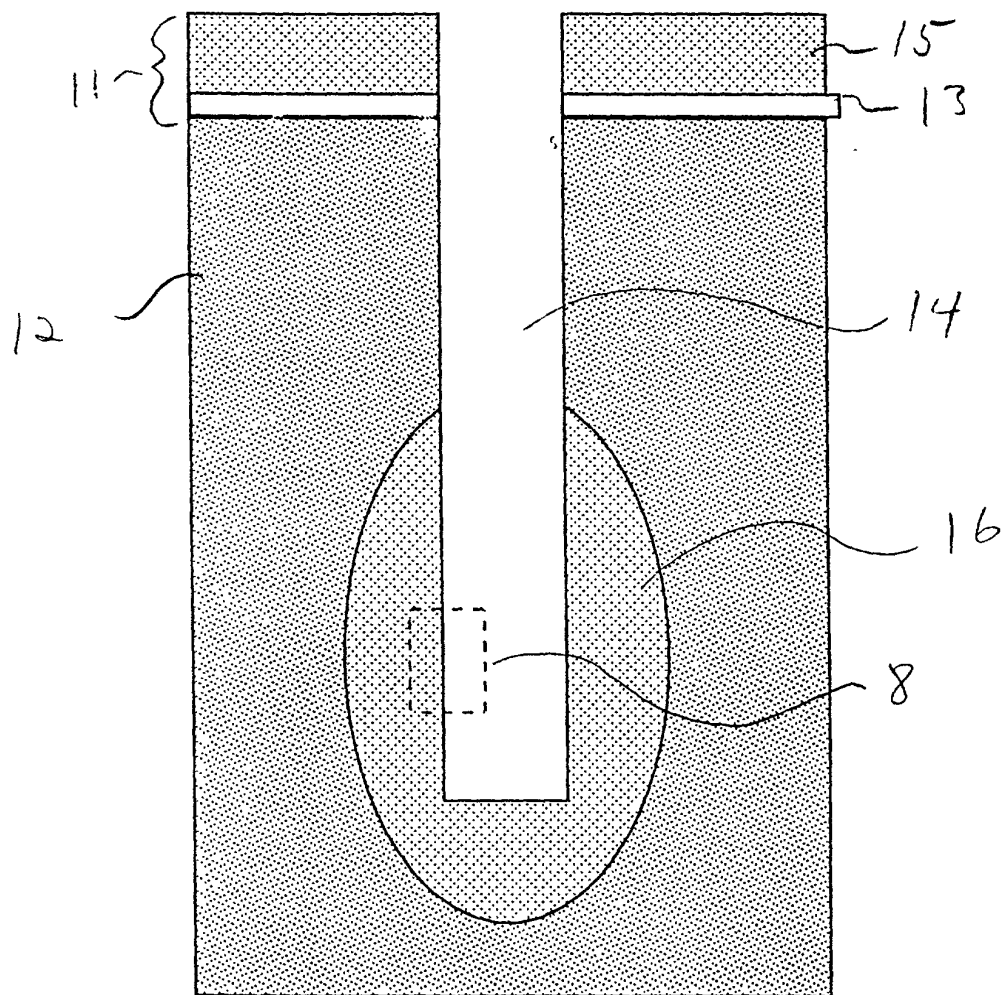


FIG. 2

A hand-drawn diagram of a rectangular structure. The structure is divided into two main horizontal sections. The top section is a large rectangle with a dashed border, labeled '14' in the center. The bottom section is a smaller rectangle filled with a dense stippled pattern, labeled '16' in the center. To the left of the structure, there are three dimension lines with curly braces: the top dimension is labeled '8', the middle dimension is labeled '18', and the bottom dimension is labeled '12'. A small tick mark is visible on the right side of the dashed rectangle.

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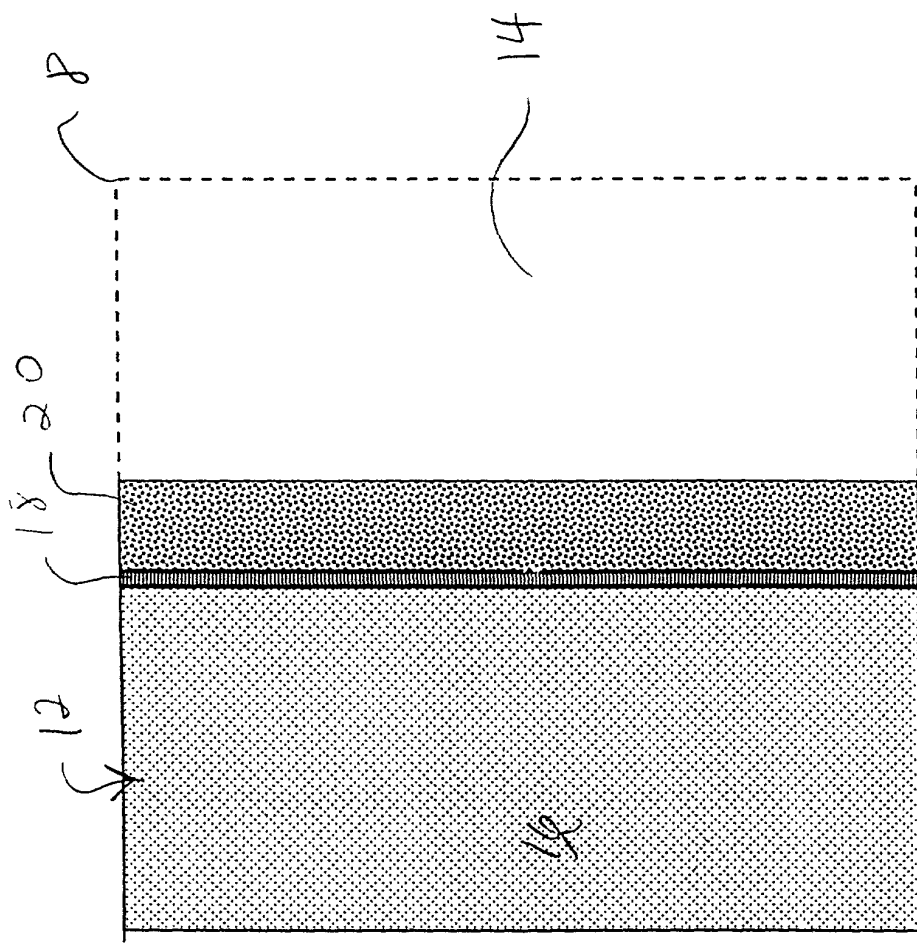


FIG. 4

FIG. 5

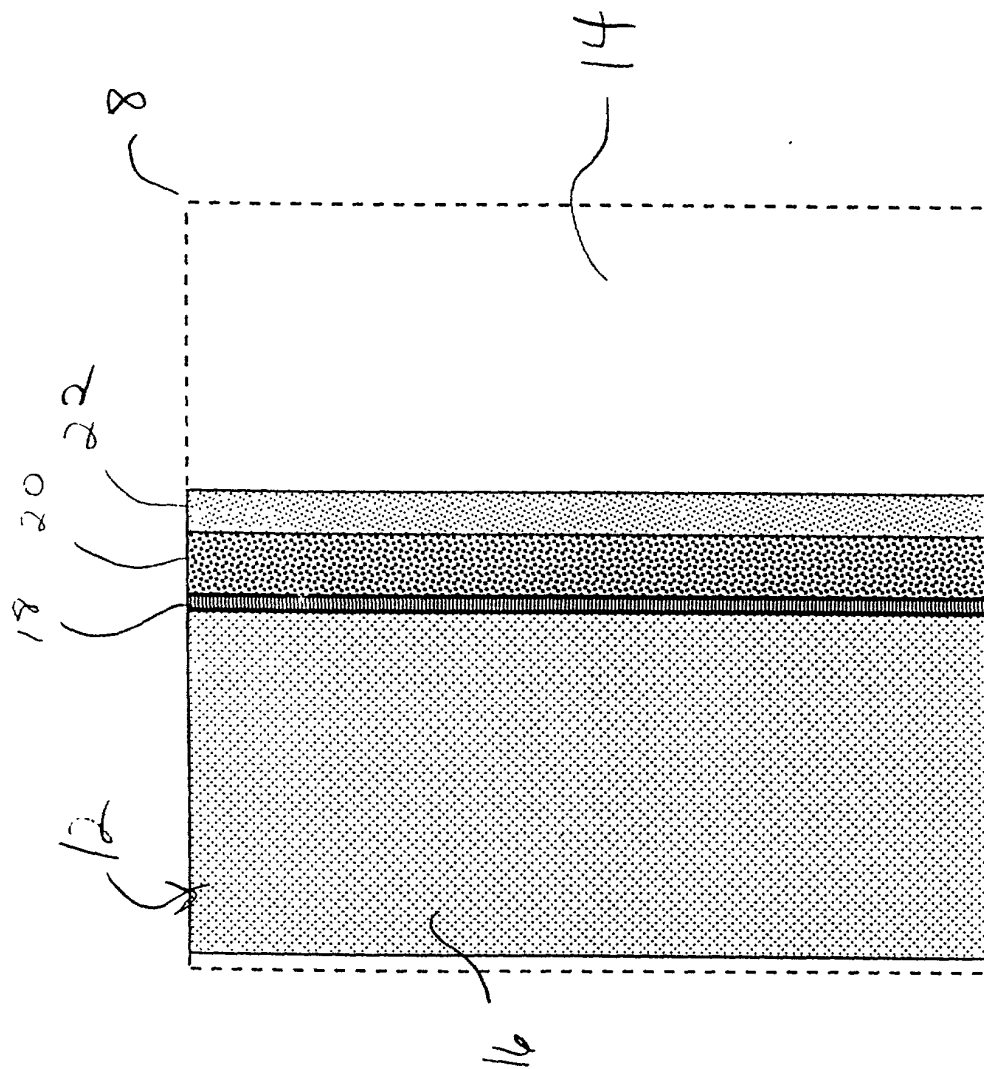


FIG. 5

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe we are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR FORMING CRYSTALLINE SILICON NITRIDE

the specification of which
 X is attached hereto, and
 was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable)

Listing of named inventor(s): Rajarao JAMMY; Philip L. FLAITS; Philip E. BATSON; Hua SHEN; Yun Yu WANG

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Priority claimed

(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

I hereby claim the benefits under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status)
(Application Serial No.)	(Filing date)	(patented, pending, abandoned)
(Application Serial No.)	(Filing date)	(Status)
(Application Serial No.)	(Filing date)	(patented, pending, abandoned)

00579 00579 00579

Full name of third
inventor Philip E. BATSON

Inventor's signature _____

~~Batson~~ Philip E. Batson

Date _____

7/26/99

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Full name of fourth
inventor Hua SHEN

Inventor's signature _____

Hua

Date _____

7/14/99

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Citizenship China

Post Office Address 1C Hudson View Dr. Beacon, NY 12508

Full name of fifth
inventor Yun Yu WANG

Inventor's signature _____

Yun-Yu Wang

Date _____

7/14/99

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Poughquag

Yun Yu Wang

009450-3637650